Crystal Image through
Imaging Innovation

PIXELPLUS

Brief Datasheet

1/4.5” NTSC/PAL CMOS Image Sensor with 640x480 Pixel Array

PC7090K

Rev 0.0

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▶ Features

▷ 648 x 488 Effective pixel array with
RGB bayer color filters and micro-lens.

▷ Power supply :
AVDD/HVDD/CVDD=3.3V

▷ Input. Clock Frequency : 27MHz

▷ Output format & Interface
◆ Composite Output mode
- CVBS (NTSC/PAL)

◆ Analog/Digital Concurrent Output mode
- ITU-R.BT656 (720x240/288)

▷ Image processing on chip
lens shading, gamma/defect/color correction
NR (2D noise reduction), color interpolation,
edge enhancement, brightness, contrast
auto black level, auto white balance
auto exposure control
and back light compensation

▷ I2C master include

▷ Horizontal / Vertical mirroring

▷ Automatic flicker cancellation

▷ Software Reset

▷ Crystal input support

▷ On chip regulator for Core

▷ CSP Package type supports

Pixel Size	5.50 um x 5.50 um
Effective Pixel Array	648 (H) x 488 (V)
Effective Image Area	3.26 mm x 2.52 mm
Optical Format	1/4.5 inch
Input Clock frequency	27Mhz
Frame Rate	60 field / sec @ NTSC 50 field / sec @ PAL
Dark Signal	TBD [mV/sec] @ 60℃
Sensitivity	TBD [V/Lux.sec]
Power Supply	AVDD : 3.3V HVDD : 3.3V CVDD : 3.3V
Power Consumption	TBD mW @ Dynamic_NTSC TBD mW @ Dynamic_PAL
	TBD uW @ Standby
Operating Temp. (Fully Functional Temp)	-40 ~ 105 [℃]
Dynamic Range	TBD [dB]
SNR	TBD [dB]

[Table 1] Typical Parameters

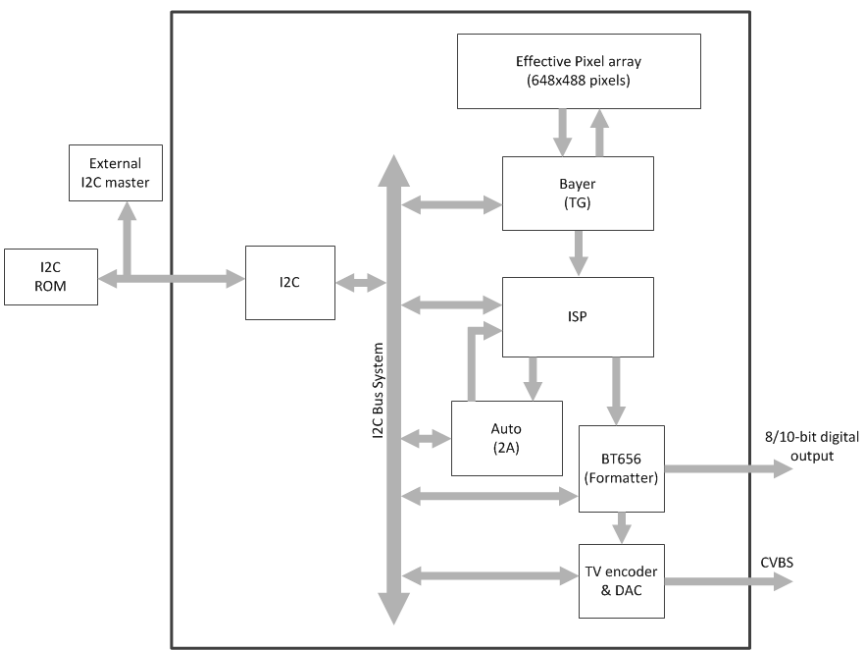
▶ General Description

The PC7090K is 1/4.5-inch CMOS image sensor. It has a Bayer sensor camera with effective pixel array of 648 (width) x 488 (height). The PC7090K can generate 10-bit YUV422 data (ITU-R BT656) at maximum frame rate of 60 field/sec with 27 MHz output clock frequency for NTSC mode. On-chip sensor functions are controllable through I2C interface.

▶ Chip Architecture

PC7090K has 648 x 488 effective pixel array and includes column/row driver circuits for reading out the pixel data progressively. correlated double sampling (CDS) circuit reduces noise generated from various sources, which mainly is resulted from process variations. Pixel output level is compared with the reset level of the pixel, and the difference between the two levels is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital form one line at a time processing blocks to produce YCbCr 4:2:2 output data. Image signal processing includes operations such as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. BT656 formatter supports 10-bit digital output and TV encoder supports CVBS analog output.

Internal functions and output signal timing can be changed by modifying registers directly via 2-wire serial interface called I2C or by programming the internal/external ROMs which contain device settings.



[Fig. 1] Block Diagram

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